REMARKS

Responsive to the Restriction Requirement, applicants hereby elect without traverse to prosecute claims 1-15 in Group I. Claims 16-33 have been canceled without prejudice.

Claims 1-15 were submitted for examination. Claims 1-15 have been rejected. Claims 1, 5, 6, and 10 have been objected to. Claims 1, 4-6, 9-11, 14, and 15 have been amended.

No new matter has been added.

Reconsideration and reexamination of the above-referenced patent application, is respectfully requested.

Claim Objections

Claims 1 and 6 have been objected to. Claims 1 and 6 have been amended. The objections have been overcome.

35 USC §112

Claims 1 and 6 have been rejected as having insufficient antecedent basis. Claims 1 and 6 have been amended. The 112 rejections have been overcome.

35 U.S.C. § 103(a) Rejection – Poisner & Elkhoury

Claims 1-15 were rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,983,354 to Poisner et al. ("Poisner") in view of U.S. Patent No. 6,205,507 to Elkhoury et al. ("Elkhoury").

Independent claim 1 recites in part:

"setting a memory area used by a bus master device as write-through cacheable,

the memory and the bus master device being in a computer system;

not setting a bus master status bit (BM_STS) for any memory read operation associated with the memory area by the bus master device; and

keeping a processor in the computer system in a low power state during the memory read operation."

(Emphasis added.)

The Examiner stated in the Office Action that Poisner teaches a requirement for placing a processor into a low power state (C3 state) is to make sure that no bus master device is communicating with the main memory because in the C3 state the processor will be unable to maintain cache coherency with the main memory. The Examiner further stated that Elkhoury teaches setting the memory as non-cacheable so that the snoop routine from the processor will not be executed. This would allow placing the processor into the low power state of C3 and at the same time not setting the bus master status bit.

Applicant submits that neither Poisner nor Elkhoury teaches setting a memory area as write-through cacheable and not setting a bus master status bit for a memory ready operation associated with the memory area by a bus master device, as claimed in claim 1.

Applicant submits that, at least for the above reason, the 103(a) rejection has been overcome and that claim 1 is patentable over Poisner in view of Elkhoury. Since claims 2-5 depend from and further limit claim 1, they are also patentable over Poisner in view of Elkhoury.

Applicant further submits that, at least for the same reason provided for claim 1, claims 6 and 11 and their corresponding dependent claims are also patentable over Poisner in view of Elkhoury.

CONCLUSION

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call David Tran at (408) 765-4692.

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due.

Respectfully submitted,

Date: March 4, 2005

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